27-29 to clearly number the claims and remedy the indefiniteness problem.

Withdrawal of the §112 rejections is solicited.

The Official Action rejected claims 1, 3, 8, 10-11, and 13-14 under §102 as anticipated by AOKI et al. 6,229,188.

The Official Action rejected claims 2, 4, and 12 under §103 over AOKI et al. in view of VO et al. 5,424,226.

The Official Action rejected claim 9 under §103 in view of AOKI et al. and VO et al. in further view of WOLF (ISBN 0-961672-4-5).

All of the rejections rely on the disclosure of AOKI et al. As AOKI et al. is not believed to teach the features for which it was offered, none of the rejections are believed to be viable. Accordingly, withdrawal of all of the rejections and allowance of all the claims are respectfully requested.

Turning to claim 1 first, AOKI et al. is not seen as disclosing the recited channel region in either of Figure 1B or Figures 5.

In Figure 1B, region 2A is correctly identified as the channel region. Column 2, lines 20-40 indicate that region 2A is an epitaxial growth layer having an impurity doping concentration lower than that of the substrate 1 (note that there is no disclosure that the impurity type is different from that of substrate 1).

Claim 1 recites "a channel region of...a first

conductivity type being selectively provided in a semiconductor region of a second conductivity type...".

The Official Action offers substrate 1 of Figure 1B as the recited semiconductor region of a second conductivity type. However, there is no disclosure of the substrate and epitaxial layer 2A being of different conductivity types. Note that in column 2, lines 34-36, it is disclosed that the impurity of the second epitaxial layer is opposite to that of the substrate. From this it appears that the impurity type of the substrate 1 is the same as the impurity type of epitaxial layer 2A.

Even apart from this, the recitation is that the channel region is provided **in** a semiconductor region of a second conductivity type. Region 2A comes from layer 2A and is provided **on** substrate 1 not **in** any semiconductor region.

Claim 1 next recites that the channel region is underlying a gate insulating film. The Official Action offers regions 2B (gate insulating film) and 5 (gate oxide film).

Claim 1 concludes by reciting that "an interface of said channel region to said gate insulating film lies at a lower level than an upper surface of said semiconductor region."

The Official Action points to column 2, lines 30-31 for disclosure of this recitation. That portion of column 2 reads: "A MOSFET shown in FIG. 1B has two epitaxial growth layers of different impurity doping concentration and different thickness provided on a substrate 1 of high impurity doping concentration.

This structure provides a buried channel type device." Applicant does not see that the referenced passage discloses the claim recitation.

Indeed, any interface between AOKI et al. regions 2B/5 and 2A necessarily lies at a higher level, not a lower level, than an upper surface of the semiconductor substrate 1 as channel region 2A as well as regions 2B and 5 are all completely above substrate 1.

Therefore, as to Figure 1B of AOKI et al., the anticipation rejection is not believed to be viable.

The Official Action also offers Figures 5 of AOKI et al. as anticipatory.

For the recited channel region, the Official Action offers "the region underneath 9 in Figure 5" in line 3 of paragraph 5, page 3. The Official Action appears to mean that, during FET operation, a channel region will form within substrate 1 in the region underneath 9. The Official Action offers substrate 1 as the recited semiconductor region of a second type.

Of course, as noted above, claim 1 recites "a channel region of...a **first** conductivity type being selectively provided in a semiconductor region of a **second** conductivity type...". If the channel region is formed in substrate 1 underneath 9, then the channel region and the substrate clearly have the same conductivity type.

However, the Official Action is not entirely clear on

this point as, for the recited channel region, the Official Action also offers "the epitaxial doped region 9 in Figures 5" in line 6 of paragraph 5, page 3. The Official Action offers substrate 1 as the recited semiconductor region of a second type.

The relative impurity types of the substrate 1 and region 9 are not disclosed.

Claim 1 next recites that the channel region is underlying a gate insulating film. The Official Action offers region 10 (gate oxide film) for this recitation.

Claim 1 concludes by reciting that "an interface of said channel region to said gate insulating film lies at a lower level than an upper surface of said semiconductor region."

The Official Action again points to column 2, lines 30-31 for disclosure of this recitation. This passage concerns Figure 1B not Figures 5.

In any event, any interface between AOKI et al. regions 9 and 10 (in Figure 5J) necessarily lies at a higher level, not a lower level, than an upper surface of the semiconductor substrate 1 as region 9 as well as region 10 are both completely above substrate 1.

Therefore, also as to Figures 5 of AOKI et al., the anticipation rejection is not believed to be viable.

Claim 8 was also rejected over AOKI et al. Figures 1 and 5.

As noted above, applicant cannot find disclosure that

offered channel region 2B or 9 is of a first conductivity type whereas substrate 1 is of a second conductivity type.

Also as noted above, any interface of a channel region to a gate insulating film in AOKI et al. lies at a **higher level**, not a lower level, than an upper surface of the AOKI et al. substrate 1 (offered as the recited semiconductor region).

Accordingly, the anticipation rejection as to claim 8 is also not believed to be viable.

Claim 11 has been amended consistent with the disclosure of at least application Figure 2D. Claim 11 recites a semiconductor wafer comprising an impurity diffused region of a first conductivity type being selectively provided in a semiconductor region of a second conductivity type, with an oxide film overlying the impurity diffused region and with an upper surface of the semiconductor region being exposed at an upper surface of the semiconductor wafer on each end of the oxide film. The claim further recited wherein an interface of said impurity diffused region to said oxide film lies at a lower level than the upper surface of said semiconductor wafer.

As amended, the claim is believed to be patentable.

Claim 28 corresponds to the second originally-filed claim 6 and recites:

A semiconductor wafer comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial layer of the first conductivity type

overlying said semiconductor substrate;

a well region of a second conductivity type selectively provided in said epitaxial layer; and

an impurity diffused channel region being selectively provided in said well region, and said impurity diffused channel region being doped with an impurity of the first conductivity type which is for adjustment to a threshold voltage of a depletion type lateral field effect transistor,

wherein said upper surface of said impurity diffused channel region lies at a lower level than said upper surface of said well region.

This claim was not examined. However, the claim is believed to be patentable over the applied art.

Accordingly, all of these independent claims are believed to be patentable. The dependent claims are therefore believed to be patentable at least for depending from an allowable independent claim.

Further, dependent claims 2 and 12 have been amended to recite, "wherein said semiconductor region comprises a well region of the second conductivity type selectively provided in a semiconductor substrate of the first conductivity type." These recitations, as well as those of independent claim 4 are believed to be non-obvious over the applied art.

The Official Action states that AOKI et al. "do not necessarily teach the further limitations of claims 2 casu quo

claim 12." The Official Action stated that it would have been obvious to include the further recitation (the semiconductor region comprising a well region selectively provided in a semiconductor substrate) since VO et al. teach a depletion-mode NMOS within a CMOS requiring the inclusion of a well.

Applicant respectfully disagrees. The Official Action cannot just pick and choose features from two references and add them together in view of the present application. The issue is whether one of skill would modify AOKI et al. in view of VO et al. so as to result in the recited invention. Applicant believes that it is clear that no motivation exists.

See that AOKI et al. utilize an epitaxial growth to provide further layers on top of the substrate. The question is how the teachings of VO et al. might be applied to this structure. VO et al. teach (Background and Summary sections) a process of fabricating a depletion mode NMOS transistor by extending the source and drain regions of the transistor into the gate area, i.e., by extending the source and drain regions into the gate area by two separate n-wells. The key parameter in the VO et al. approach is the separation distance between the n-wells under the gate area as the lateral diffusion of the n-well plus the depletion region when a voltage is applied across the source and drain will form a conduction channel under the gate.

Thus, the VO et al. teaching involves two wells and controlling a separation distance therebetween so as to obtain

several depletion mode devices with different threshold voltages on the same chip.

VO et al. do not appear to have any teachings which lend themselves to a device using an epitaxial grown channel region (e.g., 2A of AOKI et al. Figure 1B or 9 of Figure 5J).

Further, how would the method steps of VO et al. be brought into the AOKI et al. method?

See that VO et al. wells are created early in the process by phosphorus implantation (Figure 1c). Note that AOKI et al. teach epitaxial growth for providing the 2A channel region and the 2B gate insulation film. This would result in the "modified" AOKI et al. device having a channel region sitting atop, but not in, a well region. Such a device is not seen as meeting all the recitations of these claims.

Claim 4 recites a well region for a depletion type lateral field effect transistor where that well region of a second conductivity type being selectively provided in a semiconductor substrate. However, the claim also recites that the well region has an upper surface and including an impurity diffused region which is selectively provided in the well region. The modified AOKI et al. device would have the channel region on top of the well and not in the well region as recited.

Also the modified AOKI et al. device would not meet the recitation that the upper surface of the impurity diffused region lies at a lower level than the upper surface of said well region,

the impurity region being grown on top of the well region.

These comments concerning the structure of a modified AOKI et al. device also apply to the WOLF teachings.

Accordingly, reconsideration and allowance of all the pending claims are respectfully requested.

Note that the recitations of claims 30-40 are believed to be independently patentable.

As per claim 30, the art does not show a depletion type lateral MOS field effect transistor wherein the channel region, provided in the semiconductor region, comprises throughout the channel region a first concentration of first impurities of the second conductivity type and a higher second concentration of second impurities of the first conductivity type whereby the channel region is of the first conductivity type, and the semiconductor region comprises a third concentration of the first impurities of the second conductivity type, the third concentration being higher than the first concentration.

As per claim 31, the prior art does not show the channel region of claim 1, wherein, the channel region comprises a first concentration of first impurities of the second conductivity type and a higher second concentration of second impurities of the first conductivity type whereby the channel region is of the first conductivity type, and the semiconductor region comprises a third concentration of the first impurities of the second conductivity type, the third concentration being

higher than the first concentration.

Also see claim 32 reciting the well region of claim 4, wherein, the impurity diffused region is a channel region, the channel region comprises a first concentration of a first impurity of the second conductivity type and a higher second concentration of the impurity of the first conductivity type whereby the channel region is of the first conductivity type, and the well comprises a third concentration of the first impurity of the second conductivity type, the third concentration being higher than the first concentration.

New independent claim 33 recites a depletion type lateral field effect transistor, comprising:

an n+-type semiconductor substrate (1) with a first impurity concentration;

an n^--type epitaxial layer (2) with a second, impurity concentration formed over the substrate, the second concentration being lower than the first concentration;

a p-well region (5) formed in the n^--type epitaxial layer with an uppermost surface of the p-well region being co-planar with an uppermost surface of the n^--type epitaxial layer; and

an n-type channel region (6) formed in the p-well region; and

wherein an uppermost surface of the channel region lies at a lower level than the uppermost surface of the p-well region.

This structure is not seen in the prior art.

The structure of dependent claim 34, recites a gate oxide film extending over the channel region; field oxide films contacting each end of the gate oxide film and extending over the p-well; a source region contacting a first end of said channel region, said gate oxide film, and one of said field oxide films; and a drain region contacting a second end of said channel region, said gate oxide film, and another of said field oxide films.

The prior art is not seen as disclosing the transistor of claim 33, wherein, the gate oxide film extending over the channel region the n-type channel region comprises a low concentration of a p-type impurity and a higher concentration of an n-type impurity, and the p-well region comprises the p-type impurity or, wherein a concentration of the p-type impurity in the p-well is higher than the low concentration of the p-type impurity in the n-type channel region.

The recited dimensions of claim 37 have not been seen.

Claims 38-40 recite that the well region comprises a planar lower surface along an entire length of the lower surface. This supports the argument as to VO et al. and claims 2, 4, and 12.

Attached hereto is a marked-up version showing the changes made to the specification and claims. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

IN THE SPECIFICATION:

Page 5, the paragraph, beginning on line 9, bridging pages 5 and 6, has been amended as follows:

--With reference to FIG. 1I, the resist patterns 35, the gate electrodes 30a, 30b and 30c and the field oxide films 26 are used as masks for selective ion-implantation of arsenic as an n-type impurity into selected regions in the p-well region 25 and in the p+-type regions 34 at a high impurity concentration. The used resist patterns 35 are completely removed. A heat treatment is then carried out for activation of the implanted impurity, thereby to selectively form n+-type regions 36a, 36b, 36c and 36d in the p-well region 25, and n+-type regions 36e in the p+-type regions 34. The n+-type regions 36a and 36b serve as source and drain regions of the depletion type lateral MOS field effect transistor in the p-well region 25. The n+-type regions 36c and 36d serve as source and drain regions of the enhancement type lateral MOS field effect transistor in the p-well region 25. The n+-type regions 36e serve as source regions of the vertical MOS field effect transistors in the n^--type epitaxial layer 23. An inter-layer insulator 37 is entirely formed over the gate electrodes 30a, 30b and 30c, and the gate electrodes 29a, 29b and 2c as well as over the field oxide films 26. Yet another resist film is entirely applied over the inter-layer insulator 37. The resist film is then patterned by a lithography technique to form

a resist pattern [28] with openings which are positioned over contact regions of the inter-layer insulator 37.--.

Page 6, the paragraph, beginning on line 5, has been amended as follows:

--With reference to FIG. 1J, the resist pattern [28] 38 is used as a mask for selectively etching the inter-layer insulator 37 and the gate oxide films 29a, 29b and 29c to form contact holes in the inter-layer insulator 37. The contact holes are positioned over the n+-type regions 36a, 36b, 36c and 36d, as well as over the p+-type regions 34 and the n+-type regions 36e, whereby parts of the n+-type regions 36a, 36b, 36c and 36d as well as the p+-type regions 34 and parts of the n+-type regions 36e are exposed through the contact holes in the inter-layer insulator 37. The used resist pattern 38 is completely removed. An aluminum layer 39 is entirely formed over the inter-layer insulator 37 and within the contact holes, so that the aluminum layer 39 is in contact with the parts of the n+-type regions 36a, 36b, 36c and 36d as well as the p+-type regions 34 and the parts of the n+-type regions 36e. A resist film is further applied entirely over the aluminum layer 39. The resist film is then patterned by a lithography technique to form a resist pattern 40.--.

Page 21, the paragraph, beginning on line 9, has been amended as follows:

--With reference to FIG. 2I, the resist pattern 13 is used as a mask for selective ion-implantation of boron as a p-type impurity into the p-type regions 12 at a high impurity concentration. The resist pattern 13 is completely removed. A heat treatment is then carried out at 1000° C for a several [tends] tens minutes for activation of the implanted impurity to selectively form p+-type regions 14 in the p-type regions 12. The p+-type regions 14 are higher in impurity concentration than the p-type regions 12. The p+-type regions 14 serve to suppress effective operations of parasitic bipolar transistors to the vertical MOS field effect transistors. Still another resist film is entirely applied over the gate electrodes 10a, 10b and 10c, and the gate electrodes 9a, 9b and 9c as well as over the field oxide films 7a. The resist film is then patterned by a lithography technique to form resist patterns 15 which are positioned over the p+-type regions 14.--.

Page 23, the paragraph, beginning on line 9, bridging pages 23 and 24, has been amended as follows:

--With reference to FIG. 2L, the resist pattern 20 is used as a mask for selectively etching the aluminum layer 19 to form aluminum electrodes 19a, 19b, 19c, 19d, and 19e. The aluminum electrodes 19a and 19b are in contact with the source and drain regions 16a and 16b of the depletion type lateral MOS field effect transistor in the p-well region 5, so that the aluminum electrodes 19a and 19b serve as source and drain

electrodes of the depletion type lateral MOS field effect transistor. The aluminum electrodes 19c and 19d are in contact with the source and drain regions 16c and 16d of the enhancement type lateral MOS field effect transistor in the p-well region 5, so that the aluminum electrodes 19c and 19d serve as source and drain electrodes of the enhancement type lateral MOS field effect transistor. The aluminum electrode [19c] 19e is in contact with the p+-type regions 14 and the parts of the n+-type regions 16e in the p-type regions 12, so that the aluminum electrode [19c] 19e serves as a source electrode of the vertical MOS field effect transistor. The used resist pattern 20 is completely removed. A bottom electrode 21 is formed on a bottom surface of the semiconductor substrate 1.--.

IN THE CLAIMS:

1. A channel region of a depletion type lateral field effect transistor, said channel region of a first conductivity type being selectively provided in a semiconductor region of a second conductivity type, and said channel region underlying a gate insulating film,

wherein an interface of said channel region to said gate insulating film lies at a lower level than an upper surface of said semiconductor region.

Claim 2 has been amended as follows:

--2. (amended) The channel region as claimed in claim

1, wherein said semiconductor region comprises a well region of the second conductivity type selectively provided in a semiconductor substrate of the first conductivity type.--

3. The channel region as claimed in claim 1, wherein said channel region comprises a diffusion layer doped with an impurity of said first conductivity type which is for adjustment to a threshold voltage of said depletion type lateral field effect transistor.

4. A well region for a depletion type lateral field effect transistor, said well region of a second conductivity type being selectively provided in a semiconductor substrate, said well region having an upper surface and including an impurity diffused region which is selectively provided in said well region, and said impurity diffused region being doped with an impurity of a first conductivity type which is for adjustment to a threshold voltage of said depletion type lateral field effect transistor,

wherein said upper surface of said impurity diffused region lies at a lower level than said upper surface of said well region.

Claim 5 has been amended as follows:

--5. (amended) The well region as claimed in claim [1] 4, wherein said upper surface of said impurity diffused region is bounded with a gate insulating film.--

8. A depletion type lateral MOS field effect transistor comprising:

a channel region of a first conductivity type being selectively provided in a semiconductor region of a second conductivity type;

source and drain regions of the first conductivity type being selectively provided in said semiconductor region, said channel region being interposed between said source and drain regions;

a gate insulating film extending over said channel region; and

a gate electrode provided on said gate insulating film,

wherein an interface of said channel region to said gate insulating film lies at a lower level than an upper surface of said semiconductor region.

9. The channel region as claimed in claim 8, wherein said semiconductor region comprises a well region selectively provided in an epitaxial layer of the first conductivity type, and said epitaxial layer overlying a semiconductor substrate of the first conductivity type.

10. The channel region as claimed in claim 8, wherein said channel region comprises a diffusion layer doped with an impurity of said first conductivity type which is for adjustment to a threshold voltage of said depletion type lateral field

effect transistor.

Claim 11 has been amended as follows:

--11. (amended) A semiconductor wafer including:

an impurity diffused region of a first conductivity type being selectively provided in a semiconductor region of a second conductivity type; and

an oxide film overlying said impurity diffused region with an upper surface of the semiconductor region being exposed at an upper surface of said semiconductor wafer on each end of the oxide film,

wherein an interface of said impurity diffused region to said oxide film lies at a lower level than [an] the upper surface of said semiconductor wafer.--

Claim 12 has been amended as follows:

--12. (amended) The semiconductor wafer as claimed in claim 11, wherein said semiconductor region comprises a well region of the second conductivity type selectively provided in a semiconductor substrate of the first conductivity type.--

13. The semiconductor wafer as claimed in claim 11, wherein said channel region comprises a diffusion layer doped with an impurity of said first conductivity type which is for adjustment to a threshold voltage of a depletion type lateral field effect transistor.

14. The semiconductor wafer as claimed in claim 11, wherein said oxide film has a thickness of at least 5000 angstroms.

27. (new) The well region as claimed in claim 4, wherein said impurity diffused region forms a channel layer of said depletion type lateral field effect transistor.

28. (new) A semiconductor wafer comprising:

a semiconductor substrate of a first conductivity type;

an epitaxial layer of the first conductivity type overlying said semiconductor substrate;

a well region of a second conductivity type selectively provided in said epitaxial layer; and

an impurity diffused channel region being selectively provided in said well region, and said impurity diffused channel region being doped with an impurity of the first conductivity type which is for adjustment to a threshold voltage of a depletion type lateral field effect transistor,

wherein said upper surface of said impurity diffused channel region lies at a lower level than said upper surface of said well region.

29. (new) The semiconductor wafer as claimed in claim 28, wherein said upper surface of said impurity diffused region is bounded with a gate insulating film.

30. (new) The depletion type lateral MOS field effect transistor of claim 8, wherein,

the channel region, provided in the semiconductor region, comprises throughout the channel region a first concentration of first impurities of the second conductivity type and a higher second concentration of second impurities of the first conductivity type whereby the channel region is of the first conductivity type, and

the semiconductor region comprises a third concentration of the first impurities of the second conductivity type, the third concentration being higher than the first concentration.

31. (new) The channel region of claim 1, wherein,

the channel region, provided in the semiconductor region, comprises a first concentration of first impurities of the second conductivity type and a higher second concentration of second impurities of the first conductivity type whereby the channel region is of the first conductivity type, and

the semiconductor region comprises a third concentration of the first impurities of the second conductivity type, the third concentration being higher than the first concentration.

32. (new) The well region of claim 4, wherein,

the impurity diffused region is a channel region,

the channel region comprises a first concentration of a first impurity of the second conductivity type and a higher second concentration of the impurity of the first conductivity type whereby the channel region is of the first conductivity type, and

the well comprises a third concentration of the first impurity of the second conductivity type, the third concentration being higher than the first concentration.

33. (new) A depletion type lateral field effect transistor, comprising:

an n+-type semiconductor substrate (1) with a first impurity concentration;

an n^--type epitaxial layer (2) with a second, impurity concentration formed over the substrate, the second concentration being lower than the first concentration;

a p-well region (5) formed in the n^--type epitaxial layer with an uppermost surface of the p-well region being co-planar with an uppermost surface of the n^--type epitaxial layer; and

an n-type channel region (6) formed in the p-well region; and

wherein an uppermost surface of the channel region lies at a lower level than the uppermost surface of the p-well region.

34. (new) The transistor of claim 33, further

comprising:

a gate oxide film extending over the channel region;

field oxide films contacting each end of the gate oxide film and extending over the p-well;

a source region contacting a first end of said channel region, said gate oxide film, and one of said field oxide films; and

a drain region contacting a second end of said channel region, said gate oxide film, and another of said field oxide films.

35. (new) The transistor of claim 33, wherein,

the gate oxide film extending over the channel region the n-type channel region comprises a low concentration of a p-type impurity and a higher concentration of an n-type impurity, and

the p-well region comprises the p-type impurity.

36. (new) The transistor of claim 35, wherein a concentration of the p-type impurity in the p-well is higher than the low concentration of the p-type impurity in the n-type channel region.

37. (new) The transistor of claim 34, wherein,

the gate oxide film extending over the channel region has a thickness of 300 angstroms, and

the field oxide films contacting each end of the gate

oxide film have a thickness of at least 5000 angstroms.

38. (new) The channel region as claimed in claim 2, wherein said well region comprises a planar lower surface along an entire length of the lower surface.

39. (new) The well region of claim 4, wherein said well region comprises a planar lower surface along an entire length of the lower surface.

40. (new) The semiconductor wafer as claimed in claim 12, wherein said well region comprises a planar lower surface along an entire length of the lower surface.